II. Remarks

Reconsideration and re-examination of this application in view of the above amendments and the following remarks is herein respectfully requested. Claims 1, 2, 6, 13, and 17 have been amended.

After entering this amendment, claims 1-7 and 9-17 remain pending.

Claim Rejections – 35 U.S.C. § 112

Claims 1-7 and 9-17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicant has amended claims 1, 14, 15, 16 and 17 by moving the phrase "for at least one specific circuit structure described by a reference description of the digital circuit a plurality of different pre-defined implementation alternatives is known" to the preamble of the claim because this feature states a precondition for the method of the present invention. A comma has been added to further increase clarity of the claim. It is now clear that a first implementation alternative out of the plurality of the different predefined implementation alternatives is determined in step (a) of the method of claim 1.

It is further clarified that a determining performed such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified. It has been further added the wording "compared to other implementation alternatives out of the plurality of the different predefined implementation alternatives" to clearly state that one implementation alternative is

chosen that fits best for the specific circuit structure. The applicant assumes that the wording of claim 1 is now clear and, in the same time, clearly separated from the cited prior art documents. These amendments do not alter the meaning of the claim. Claims 14, 15, 16 and 17 have been amended accordingly.

The Examiner has further objected to the phrase in claim 13 "at least partially performed by a method of equivalence class refinement" as the intended meaning is unclear. The applicant has amended claim 13 by inserting the wording "wherein all internal design points, whose non-match has not yet been proven, are combined in an equivalence class". Support for this amendment may be found on page 9, lines 25 to 33 of the original filed specification.

Claim Rejections - 35 U.S.C. §103(a)

Claims 1, 4-6, 9-12, and 14-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,301,687 to Jain, et al. ("Jain '687") in view of U.S. Patent No. 6,484,292 to Jain, et al. ("Jain '292). Applicants respectfully traverse this rejection.

The Examiner states that the '687 patent describes all the features of claim 1 except a plurality of pre-defined implementation alternatives. The applicant respectfully submits that there are substantial differences in the method of the present invention with respect to the disclosures '687 and '292 of Jain. The '687 patent relates to a method for the verification and analysis of digital circuit designs (abstract) wherein a design specification is verified against a design specification from the previous design level (column 1, line 47 to 50). The '687 patent thus refers to a verification method as such,

wherein during verification the different subsequently modified specifications are used. In contrast, the present invention relates to a preparation or pre-processing method that is used to modify the reference description prior to the application of the verification of the design.

The preamble of claims 1, 14, 15, 15 and 17 has been amended to now clearly state that the method is applied prior to the verification of digital circuit and that the method provides an alternative reference description for the use in the verification at a later stage. This clearly states that the method does not relate to the verification itself but to a pre-processing that allows easier verification with a modified or alternative reference description that is used instead of the original provided reference description.

Accordingly, step c) of method 1 has been amended to now read "outputting the alternative reference description for use as a reference description in the verification of the digital circuit". The method as claimed now relates to the pre-processing and does not include the execution of the equivalence test. However, an equivalence test may be performed in the actual verification using the alternative reference description as replacement for the original reference description. The method of the invention can be applied with any verification method or equivalence test and may thus be used with the verification methods described in the '687 and '292 patents. None of the prior art documents describes a pre-processing of a reference description.

Further features has been added to step a) of the method stating that the determination of the first implementation alternative is performed "using random patent simulation" to identify the pre-defined implementation alternative as the first implementation alternative that has the largest number of equivalent design points with

digital circuit. This feature clearly states that random pattern simulation is used to identify and determine the best fitting implementation alternative out of the plurality of predefined implementation alternatives support for this amendment may be found with another on page 8 line 24 to 31 or page 14, lines 16 to 29. None of the prior art documents is based in random pattern simulation.

Claim 1 thus claims a method for the preparation or pre-processing of a reference description prior to the verification of the digital circuit. Such a pre-processing using random pattern simulation is not disclosed in the '687 '292 patents of Jain et al. Therefore the present invention is patentable of a prior art.

Furthermore, the wording of claim 1 has been amended, by moving the wording "for at least one specific circuit structure described by a reference description of a digital circuit a plurality of different pre-defined implementation alternatives is known" into the preamble of the claim to clearly state that the plurality of different pre-defined implementation alternatives is already known prior to starting the method steps of the present invention. The Examiner already states that the '687 patent does not disclose any pre-defined implementation alternatives.

However, the Examiner states that the '292 application discloses a plurality of different pre-defined implementation alternatives as prior circuit implementations. The applicant respectfully disagrees. The '292 patent discloses reusing previously verified implementations in a new design. A previously verified implementation (prior implementation, abstract) is used to replace a portion of new circuit implementation to facilitate the equivalence test. As can be seen from figure 4 a replacement of primary outputs of a specification netlist Sn by primary outputs of an implementation C0 (step

280) is only performed after a formal verification (step 276) is performed. The replacement is therefore performed during the actual verification and not in a pre-processing step. Furthermore, the implementation of the reference design is compared to a specification. Thus, no alternative reference description is formed. The '292 patent therefore differs considerably from the present application. In particularly the implementation alternatives are not pre-defined before the verification is started but are verified and collected during the verification.

The use of pre-defined implementation alternatives is therefore not disclosed in the '687 and '292 patent applications of Jain et al. Furthermore, random pattern simulation is not used for the selection of the best-fitting pre-defined implementation alternative in any of the prior art documents. The present invention is therefore patentable over both Jain et al. documents.

As claim 1 is patentable over prior art, dependant claims 2 to 13 are patentable as well. The amendments to claim 1 have been similarly made to claims 14, 15, 16 and 17 which are therefore patentable as well.

Conclusion

In view of the above amendments and remarks, it is respectfully submitted that the present form of the claims are patentably distinguishable over the art of record and that this application is now in condition for allowance. Such action is requested.

Respectfully submitted,

June 10, 2009
Date

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